Application Hint 46

High Current LDO with Foldback Current Limiting

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Introduction

At currents less than 5A, monolithic linear regulators can be used for most applications. Most manufacturers of these devices integrate current limit and thermal shutdown to prevent damage during fault conditions. For currents greater than 5A, linear supplies are dominated by controllers that allow the user to select the pass element to handle different current requirements. While these linear controllers may offer current limit, they generally don't support thermal shutdown. This requires the design to handle the maximum power dissipation and maintain an acceptable junction temperature on the pass element. For example, a 1.8V at 8A linear supply is required from a 2.5V rail.

$$\text{PowerDissipation} = (V_{IN} - V_{OUT}) \times I_{OUT}$$

$$\text{PowerDissipation} = (2.5V - 1.8V) \times 8A$$

$$\text{PowerDissipation} = 5.6W$$

That means that over the application's temperature range, the pass element must be able dissipate this amount of power and have a junction temperature less than the maximum allowable for that device. This solution will probably require 3-4 D-Pack sized MOSFETs. The problem arises when we examine power dissipation in a sustained short circuit;

$$\text{PowerDissipation} = (V_{IN} - V_{OUT}) \times I_{OUT}$$

$$\text{PowerDissipation} = (2.5V - 0V) \times 8A$$

$$\text{PowerDissipation} = 20W$$

With an estimated 2W of power dissipation, it would require 10 D-Pack sized MOSFETs to maintain an acceptable junction temperature on the MOSFETs. This would have the undesirable effect of over designing the supply, increasing cost and board size to survive a possible fault condition.

Figure 1 solves current limit power dissipation. It involves a separate control loop that "folds back" the currents during a fault condition without involving the problems of linear foldback current limiting. Linear foldback can have problems tripping current limit during start-up and returning to full load after a fault condition. These problems tend to lock up the regulator in current limited state.

Foldback Operation

U3 provides a high side reference below the supply voltage and places this voltage on the inverting pin of U2. This reference signal is compared to the MOSFET side of R1 by a comparator (U2). When the current exceeds the threshold current limit threshold, U2's inverting input voltage is greater than the non-inverting input. This causes the comparator to pull the current sense pin on U1 low. The current limit threshold calculates as follows;

$$\text{Current Limit} = \frac{V_{IN} - \left(V_{U3} \times \frac{R2}{R2 + R3}\right)}{R1}$$

$$\text{Current Limit} = \frac{2.5 - \left(1.225 \times \frac{90.9}{90.9 + 1000}\right)}{10m\Omega}$$

$$\text{Current Limit} = 10.207A$$

When the current sense pin drops 50mV below the input, the regulator turns the output off. This causes the current then to go to zero, creating a high condition on the output of the

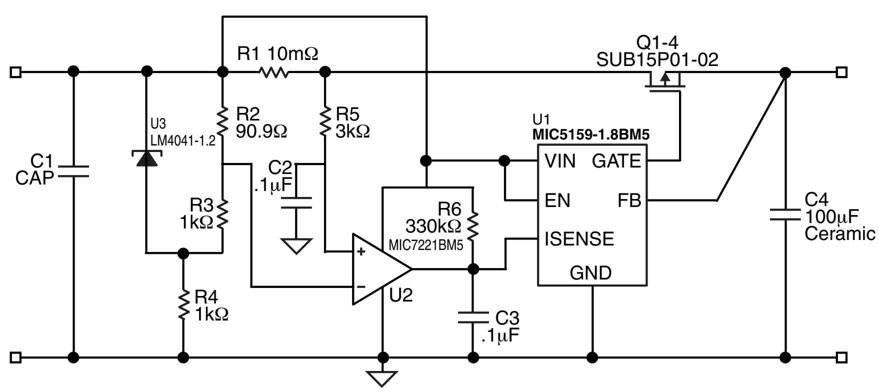

Figure 1.

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MIC5159 Foldback Current Limit

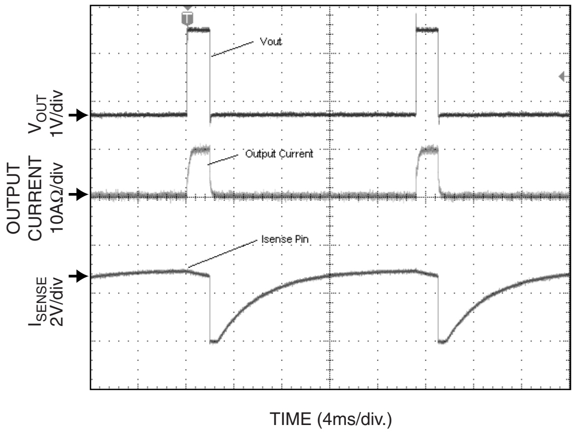

Figure 2.

comparator. The comparator is an open collector, therefore, the Isense pin charges up at the RC charge rate of R6 and C3. The output of the regulator remains off, drawing no current, until the I_{SENSE} pin charges up to 50mV below V_{IN}. After which, the output turns on. R5 and C2 provide a delay before re engaging current limit. This delay prevents the current required for charging up the output capacitors from tripping current limit prematurely. It also gives the circuit time to stabilize and determine if it can deliver the output current being requested by the load. If the load is sill too high, current limit is re-engaged. Figure 2 is an oscilloscope picture of this circuit in operation. This cycling of current, while periodically delivering maximum current, integrates over time into a lower average current. Average current can be calculated as a ratio of on to off time;

$$I_{AVG} = I_{PK} \times \frac{T_{ON}}{T_{OFF}}$$

$$I_{AVG} = 10.2A \times \frac{2ms}{17ms}$$

$$I_{AVG} = 1.2A$$

This reduced average current equates into a reduction in power dissipation. At 1.2A, the power dissipation is reduced to 3 Watts. Figures 3 and 4 show a comparison between this foldback current limiting and constant current limiting.

Foldback Current Limit vs. Constant Current Limit

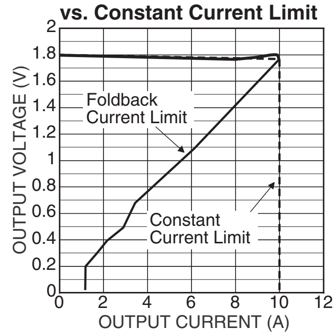

Figure 3.

Power Dissipation in Current Limit

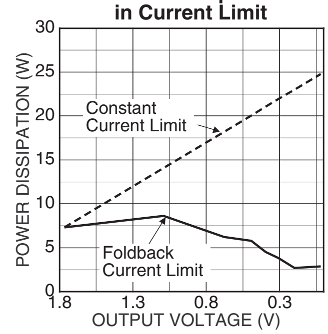

Figure 4.

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